Integrated Circuit Design Education and Research at VLSI Design and Education Center (VDEC)

Kunihiro Asada and Makoto Ikeda

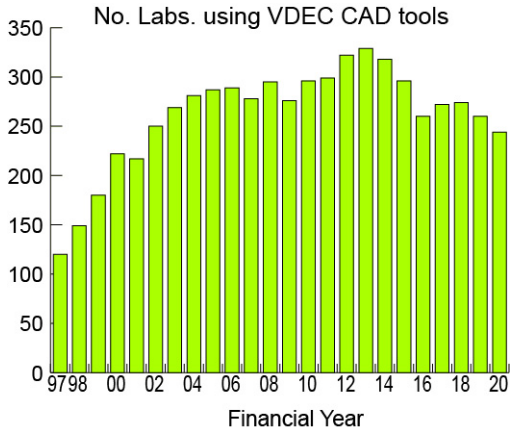
Since VLSI Design and Education Center (VDEC) was established at the University of Tokyo in 1996 and shared by users all over Japan, it has made a great contribution to the design education and research of integrated circuits at Japanese universities. In integrated circuit design in Japan before the opening of VDEC, individual researchers had to procure EDA (Electronic Design Automation) tools necessary for the design and contract for trial production, and the monetary and human costs were enormous, and as a result, few university researchers were involved in integrated circuit design research. VDEC made a one-time contract for EDA tools, supplied licenses to technical colleges and universities, and provided a shuttle service that aggregates design data and makes prototypes at low cost. It greatly reduced the burden on faculty members and students, and played a major role in expanding the base of the academic field in Japan. The number of EDA tool licenses was about 2000 when it was first opened, but it exceeded 10,000 in 2005. The number of prototype chips was less than 100 in the year of establishment, but exceeded 500 in 2006. Before the opening of VDEC, the number was less than 10 per year.

Processes that can be prototyped continue to change with the miniaturization of process rules, 0.6 μm, 0.5 μm, 0.35 μm, 0.18 μm, 0.15 μm, 90 nm, 65 nm, 45 nm, and 28 nm in addition to the very inexpensive 1.2 / 0.8 μm process that has continued since its inception. Over the 24 years since the inauguration of VDEC, more than 8,100 varieties have been prototyped. CAD training, which is a training course on how to use EDA tools, was started in 1997, and hands-on tutorial-like education for working adults and students was started in 1998, and both have been held while continuing to be updated until now.

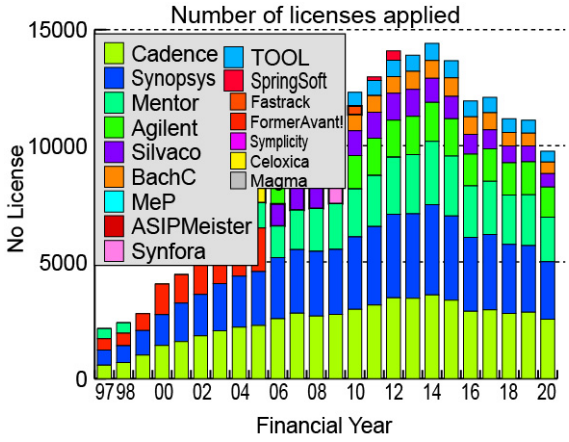
Furthermore, in 1997, the "Young People's Association for Supporting VDEC" was held as a place for information exchange between young researchers and students, and in 1998, the name was changed to "Designer's Forum", and more than 1000 people participated in the 24 meetings. In addition to exchanging information, commendations for circuits designed by students are also provided, which leads to motivation of students for research. As a result, the number of papers published related to VDEC activities has exceeded 16,000 in the past 24 years.

The award recipients made great efforts to develop human resources through integrated circuit design education and research activities at the VDEC. Award recipient Asada created the basic activity policy and served as the director of the VDEC Center for 18 years from 2000

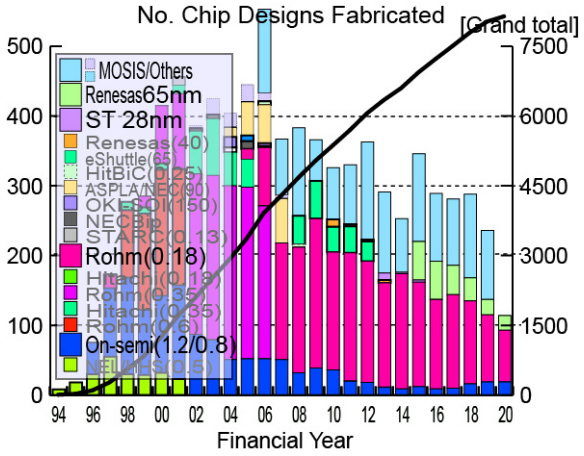
to 2018 when he retired and made a great contribution to its operation. Award recipient Ikeda was hired as an assistant at the same time as the establishment of VDEC, and after working as an associate professor, he has been a professor since 2013 and has been deeply involved in whole VDEC work. In addition, VDEC has restarted as a division due to the reorganization accompanying the establishment of the University of Tokyo System Design Research Center (d.lab) in 2019. After the reorganization, Award recipient Ikeda continues to coordinate the two major projects of the former VDEC, which is the supply of EDA licenses and the compilation of prototype data, as the head of the basic design research division of d.lab. As mentioned above, Award recipients' contributions to VDEC for more than 20 years are indispensable for the development of the integrated circuit field in Japan, and their devoted activities are considered to be an extremely large achievement that corresponds to the achievement award.



Number of laboratories using EDA tools



Number of licenses to use EDA tools



Number of prototype chip designs

(1) 浅田邦博，アナログ電子回路—VLSI 工学へのアプローチ，昭晃堂，東京，1998.
(2) 浅田邦博監修，池田誠他著，ディジタル集積回路の設計と試作，培風館，東京，2000.
(3) 浅田邦博監修，システム LSI 設計自動化技術の基礎—パブリックドメインツールの利用法 ，培風館，東京，2005.
(4) 浅田邦博編集，アナログ RF CMOS 集積回路設計 基礎編/応用編，培風館，東京，2010/2011
(5) 浅田邦博監修，はかる×わかる半導体 入門編，日経 BP コンサルティング，東京，2013.
(6) 浅田邦博，集積回路設計，コロナ社，東京，2015.
(7) 浅田邦博監修，はかる×わかる半導体 応用編，日経 BP コンサルティング，東京，2019.
(8) 池田誠，MOS による電子回路基礎，数理工学社，東京，2011.
(9) 池田誠，NANO-CHIPS 2030, Springer，ドイツ, 2020.